CORIOLIS – Analog Capabilities

SAL Bootcamp

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cnrs

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Plan

1. Introduction
2. Digital Place & Route
3. Analog Place & Route
4. State of The Toolchain
5. And Now, Let’s Have a Demo

CORIOLIS – Analog Capabilities

2025-01-25

Outline

- Why and how we do it.

Who Are We

- ✏ The CIAN Team, part of the LIP6 laboratory of Sorbonne Université.
- ✏ More that 30 years of experience in making analog designs and tools to make them.
- ✏ Analog designers are very sensitive people with lot of unique experience.

Who Are We

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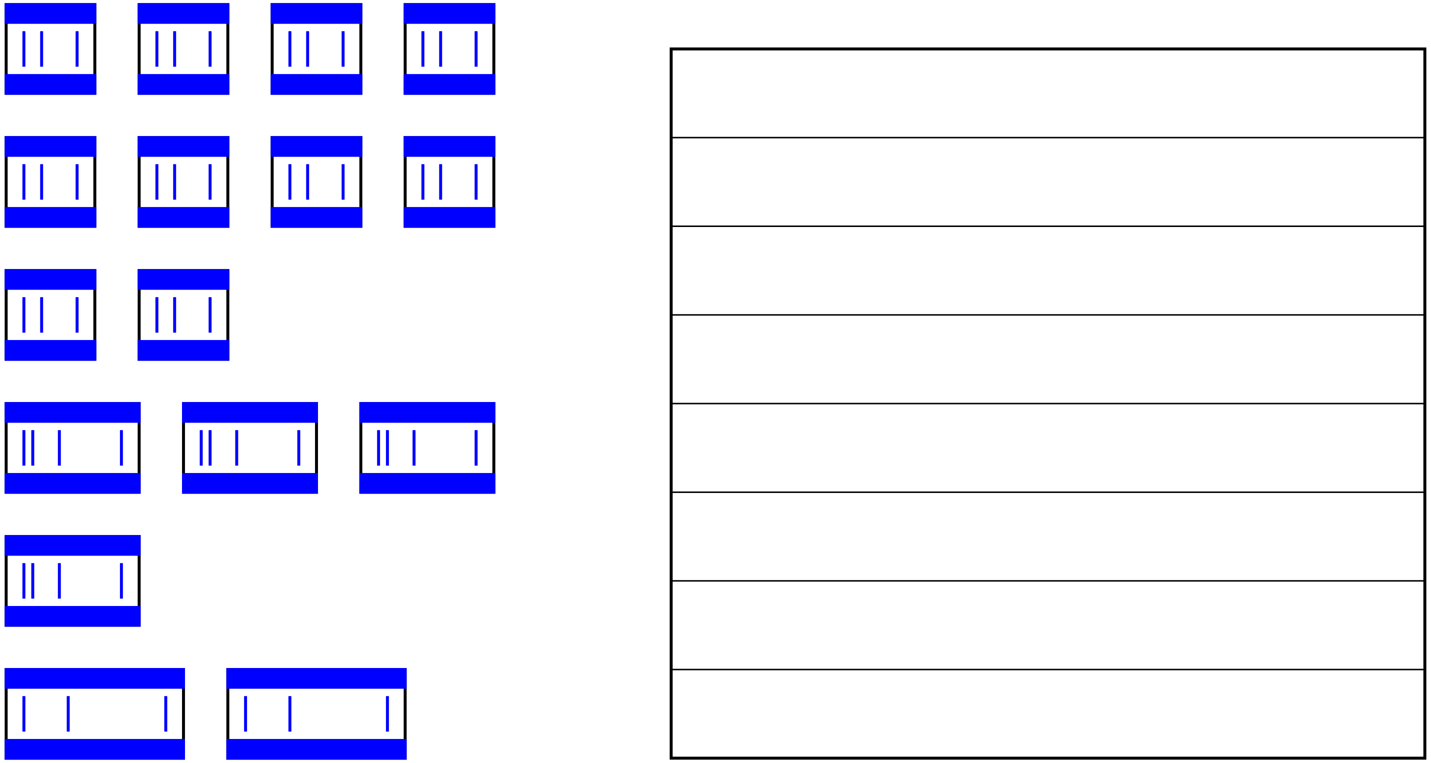
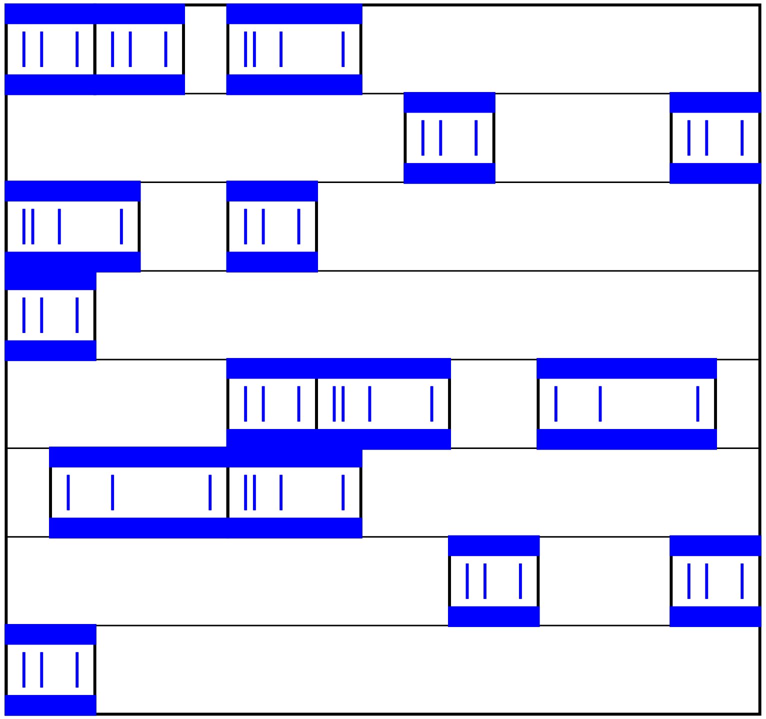
- Contrary to the others members of the team, I come from the digital design world.
- Analog designers are difficult to convince to switch to automated tools. We bolster a semi-automated one.
- Help them formalize the problem and implement a novel approach by extenting the digital P&R.

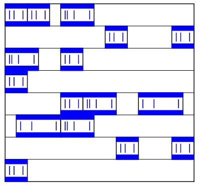
Place & Route



Place & Route

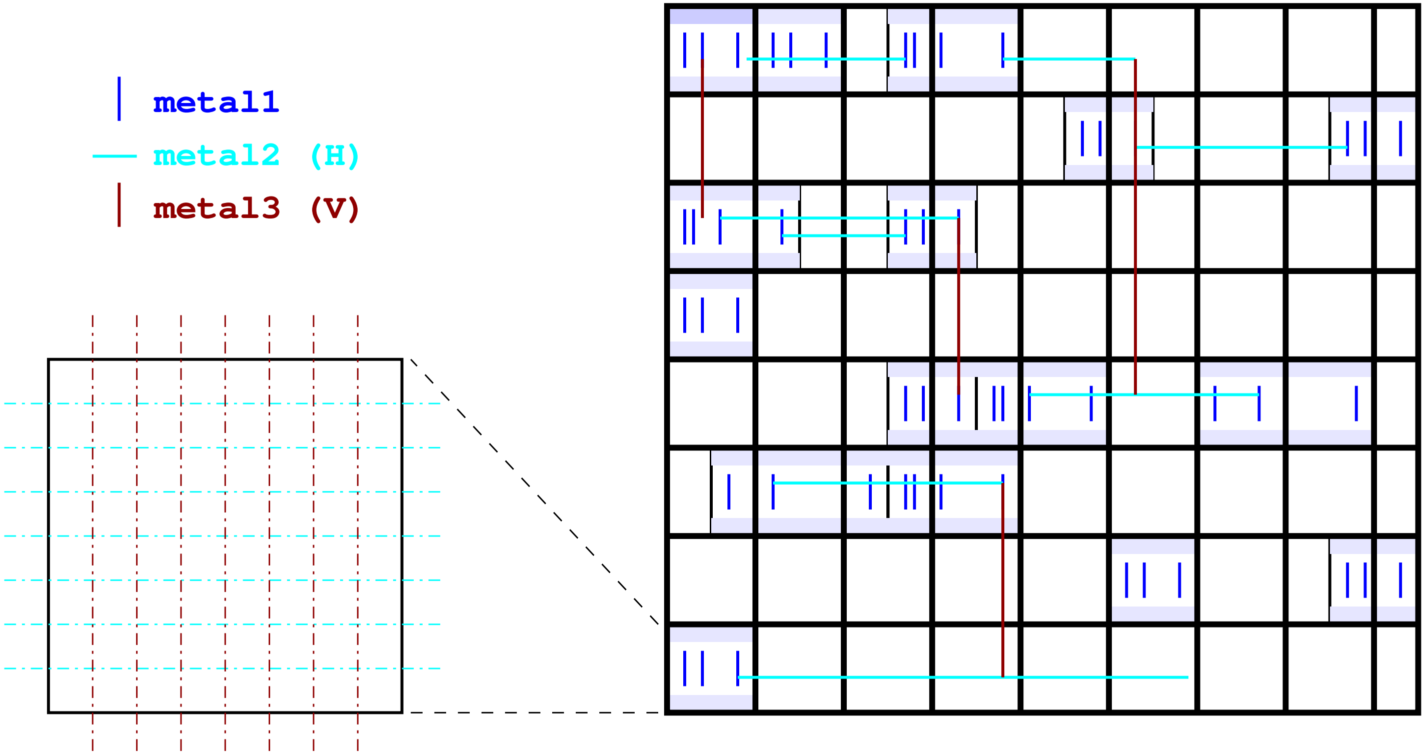


└─Place & Route



- In ASIC, the area is divided in rows (aka *slices*) of the height of a standard cells. The standard cells are then placed into those rows with the constraints:
  1. No overlap between the cells.
  2. Minimize the length of the wires connecting the cells (at this stage it is an estimate).
  3. Do not make too much wires goes through a given area as to overload the routing capacity.

Place & Route



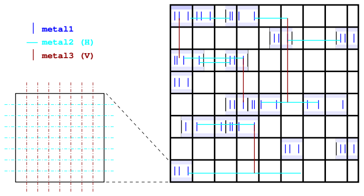
| metal1

— metal2 (H)

| metal3 (V)

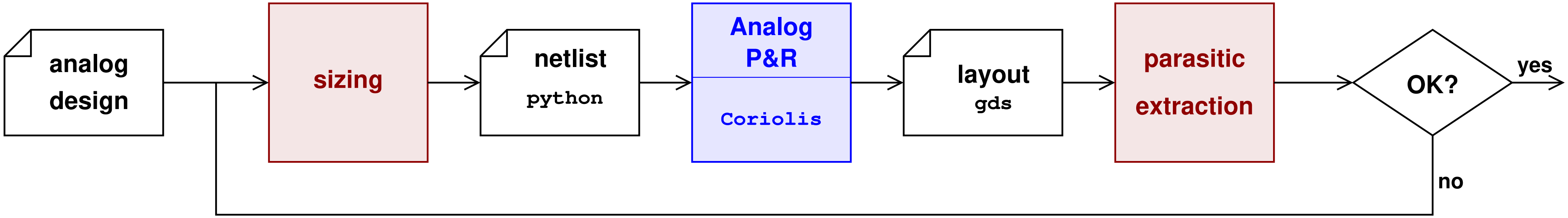
└Place & Route

Place & Route



- Draw the wires to connects the cells acording to the netlist.
- Each layer is assigned a preferred routing direction (vertical or horizontal and they alternates).
- To facilitate the work of the router, wires in a given layer are placed on regularly spaced tracks.
- So, given the track spacing and the number of layers, only a finite number of wires can go over a track.
- Placement and routing have been separated to become tractables problems, but in fact they are tightly linked. So, the better able they are to communicate, the best the result.

Overall Analog Design Flow



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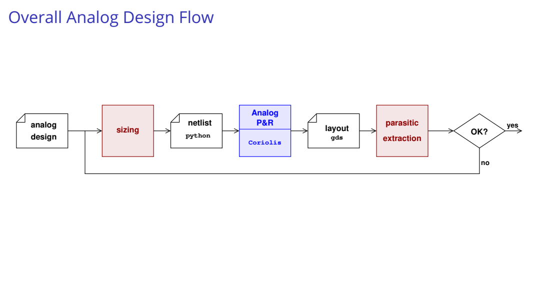
CORIOLIS – Analog Capabilities

└─Analog Place & Route

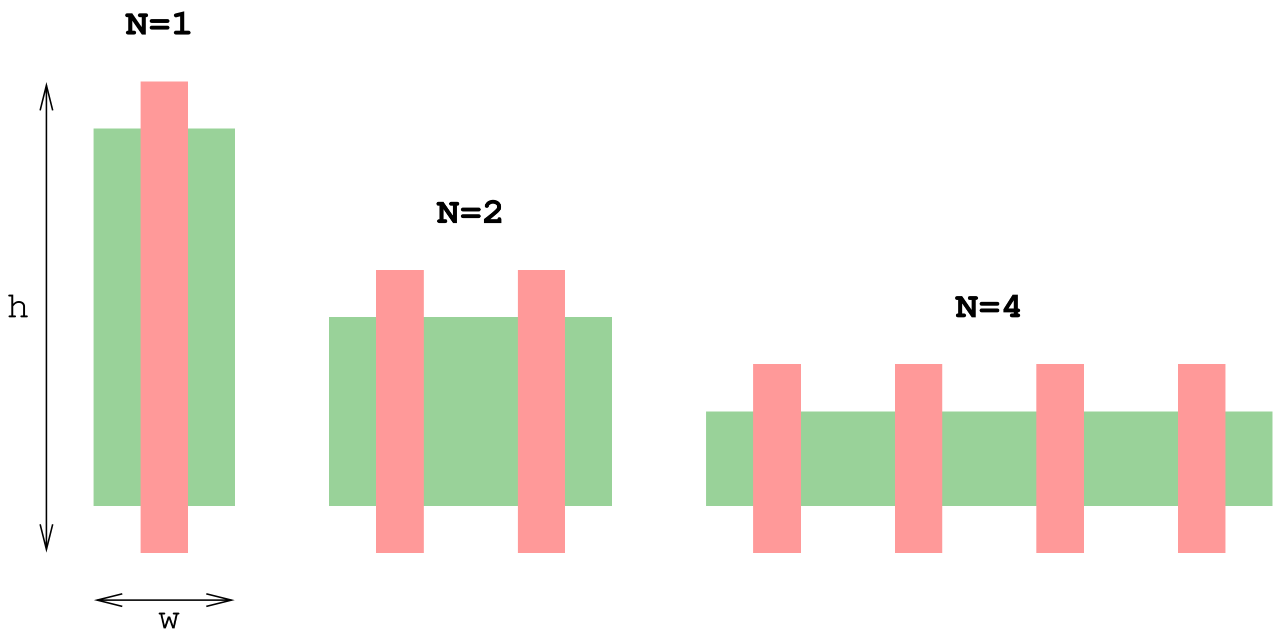
└─Overall Analog Design Flow

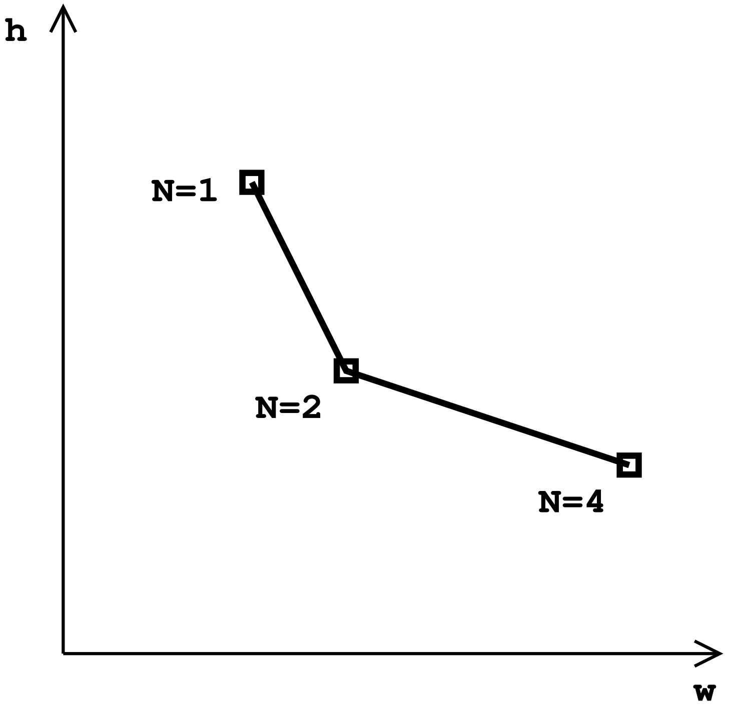


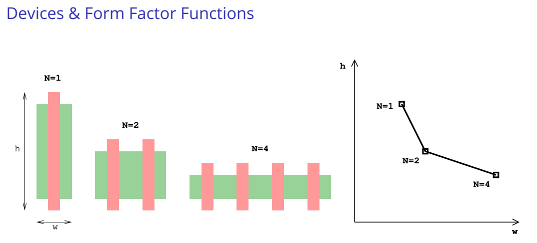
Overall Analog Design Flow

- This may not be completely accurate.
- We make the assumption that the parasitics extraction do not fundamentally change the topological characteristics of the design. That is only sligth size adjustement of the components may be needed, so the overall topology remains valid.
- CORIOLIS focus on the P&R stage.

Devices & Form Factor Functions



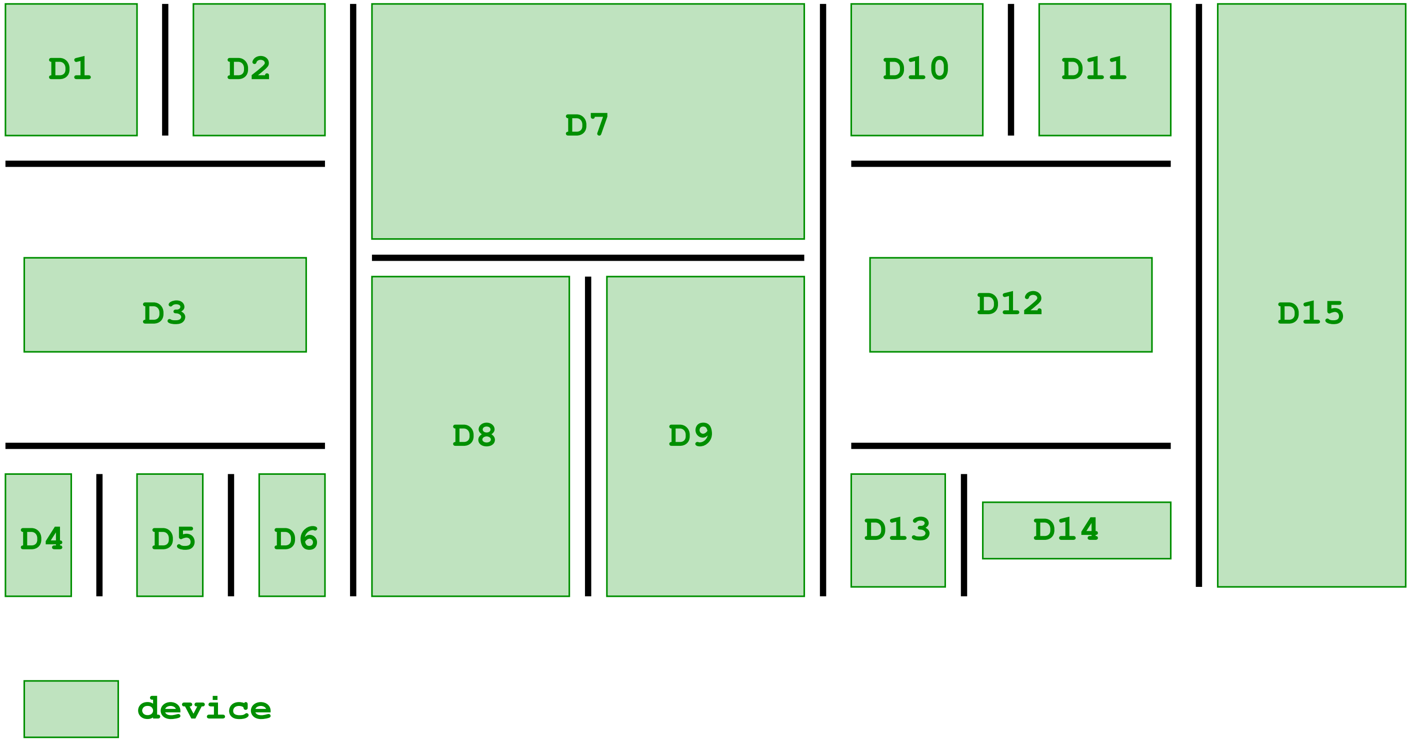




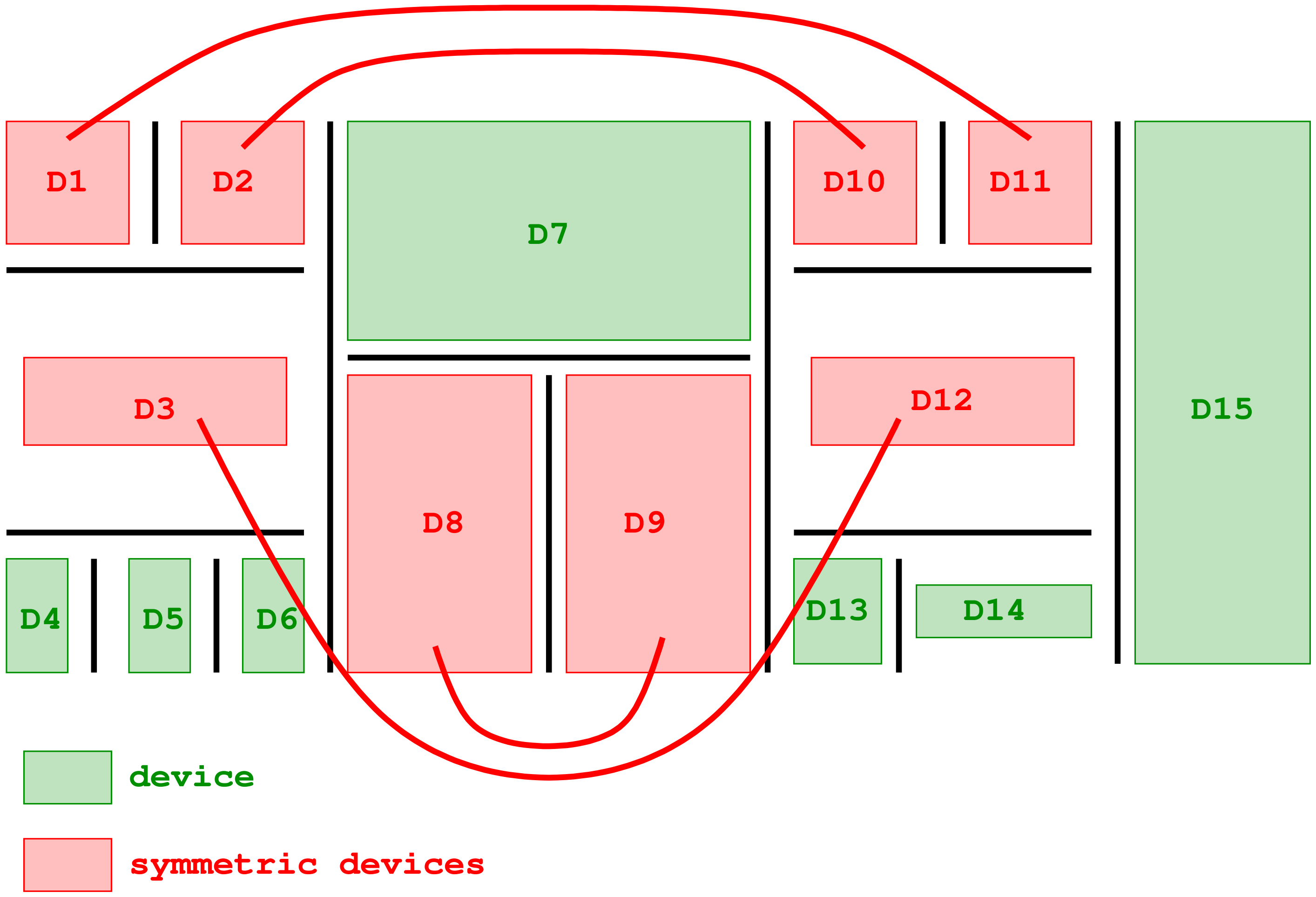
Devices & Form Factor Functions

- Devices are transistor or paired transistors, capacitors and resistors.
- The form factor function is convex.

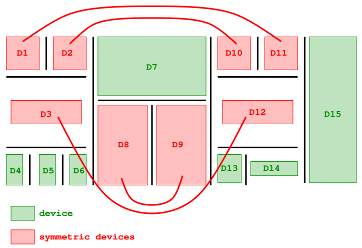
Device Assembly



Device Assembly

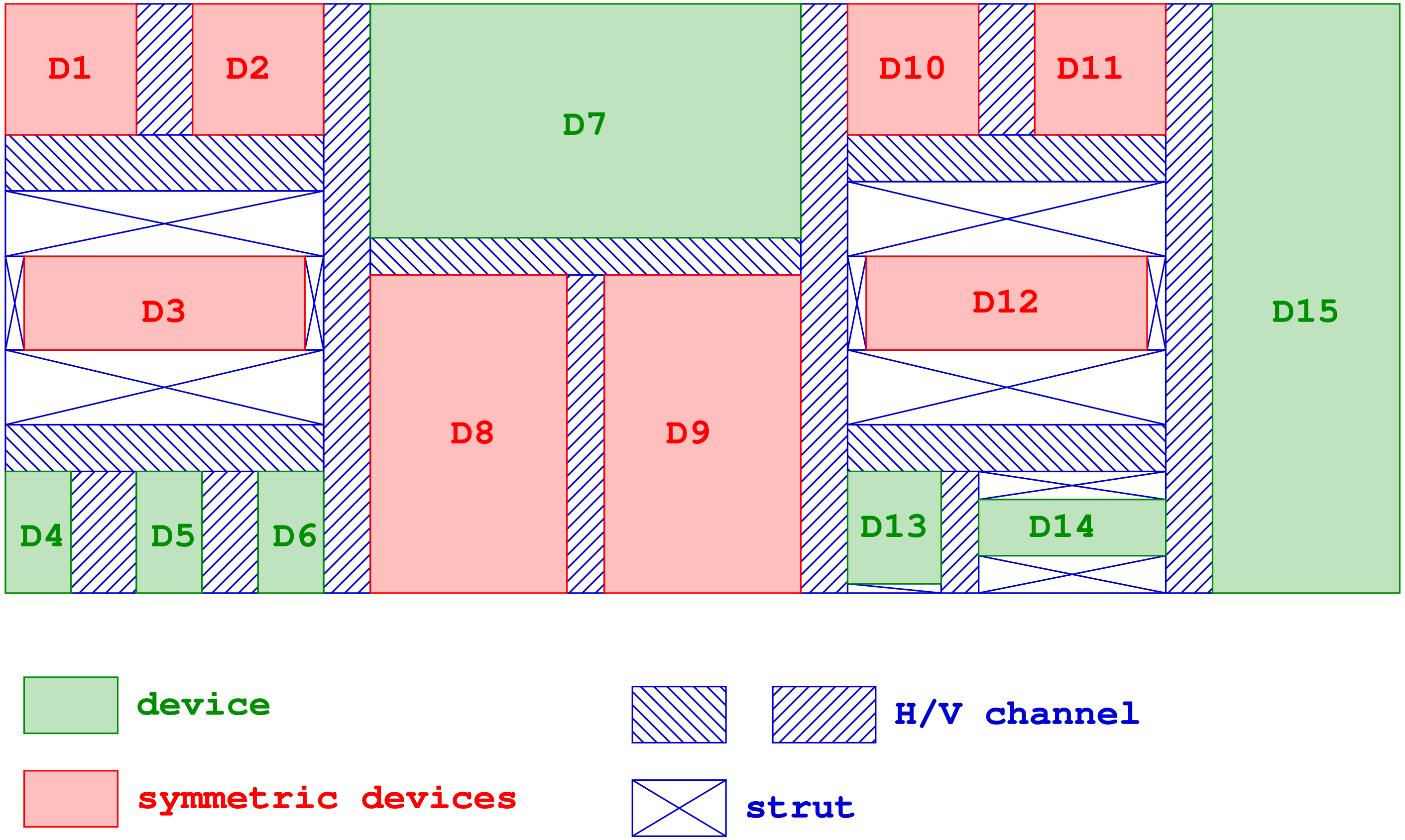


└─Device Assembly

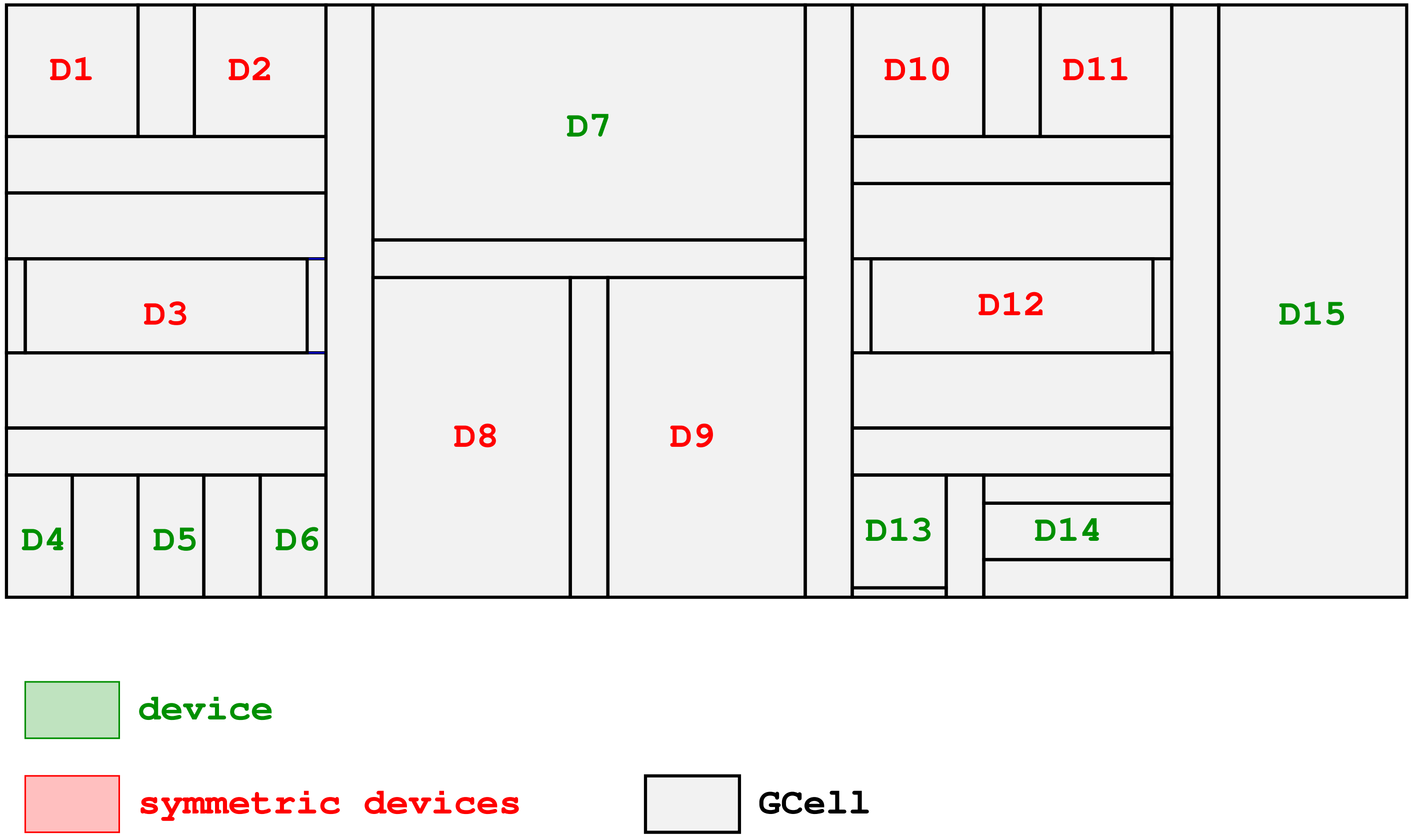


- Assembling devices : we have choosen a well know structure, a slicing tree. It is well suited to our needs.
- We support symmetry constraints. Of course, the tree must be symmetric also.

From Slicing Tree to GCells



From Slicing Tree to GCells



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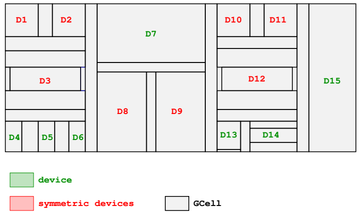
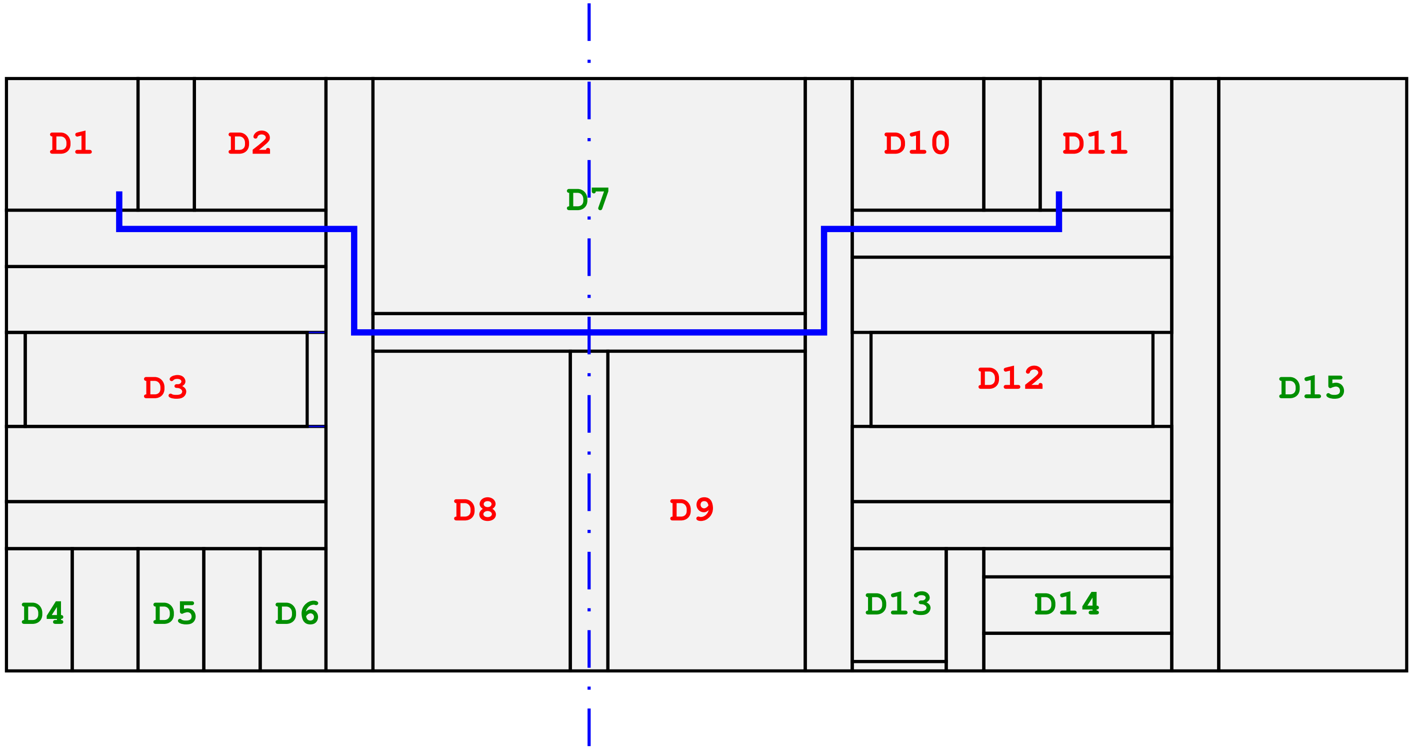
CORIOLIS – Analog Capabilities
└─Analog Place & Route
└─From Slicing Tree to GCells



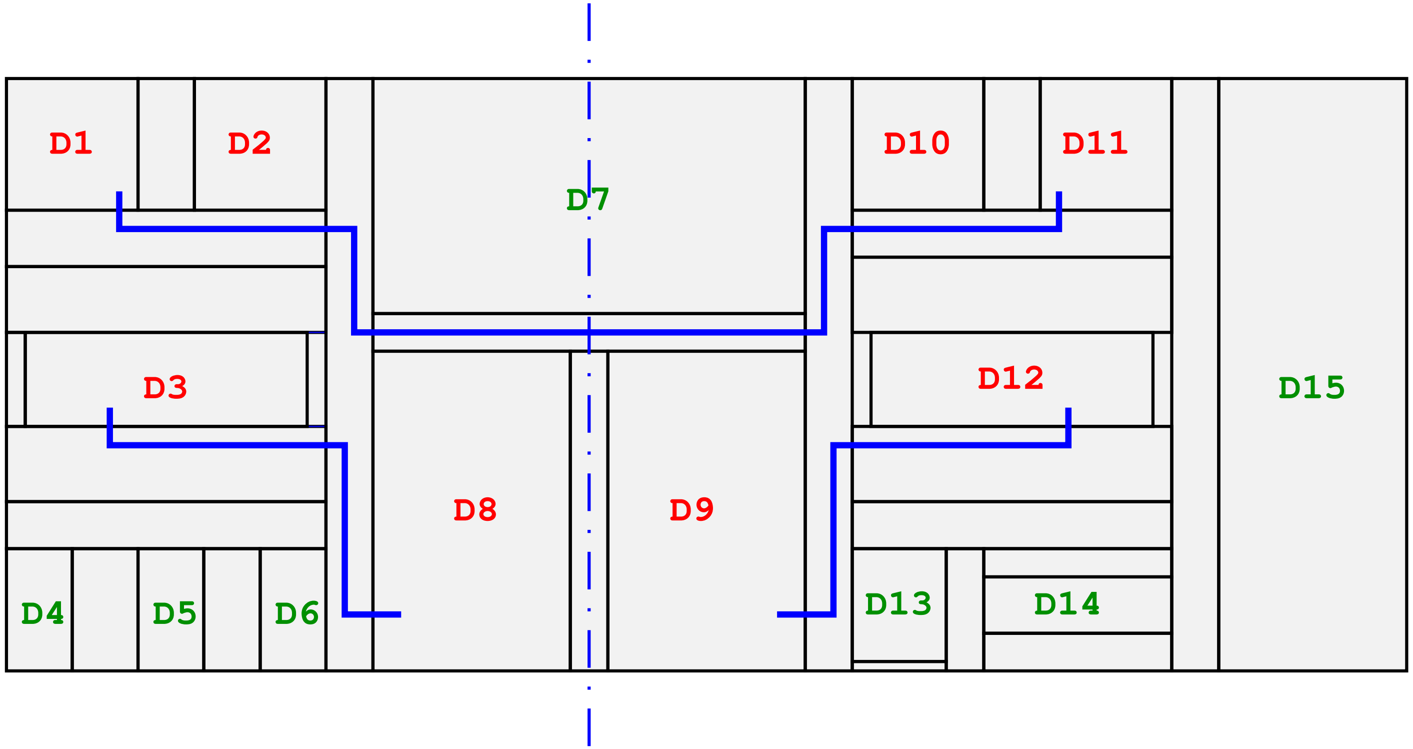
- We must not route over the active devices, consequently we have to use channels.
- So cut lines are replaced by channels for routing.
- In addition, we create struts to fill the space when a device is smaller than the area it is in. In order to center it, if need be. It can be non-centered.
- Finally all devices, channels and struts are converteds to form a complete partition of the area (it's flat).
- The GCells reflect the slicing tree.



🟩 device

🟥 symmetric devices

⬜ GCell



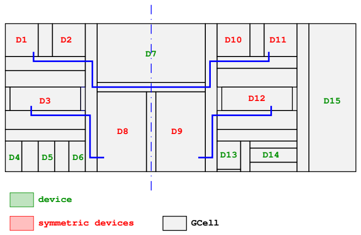
🟩 device

🟥 symmetric devices

□ GCell

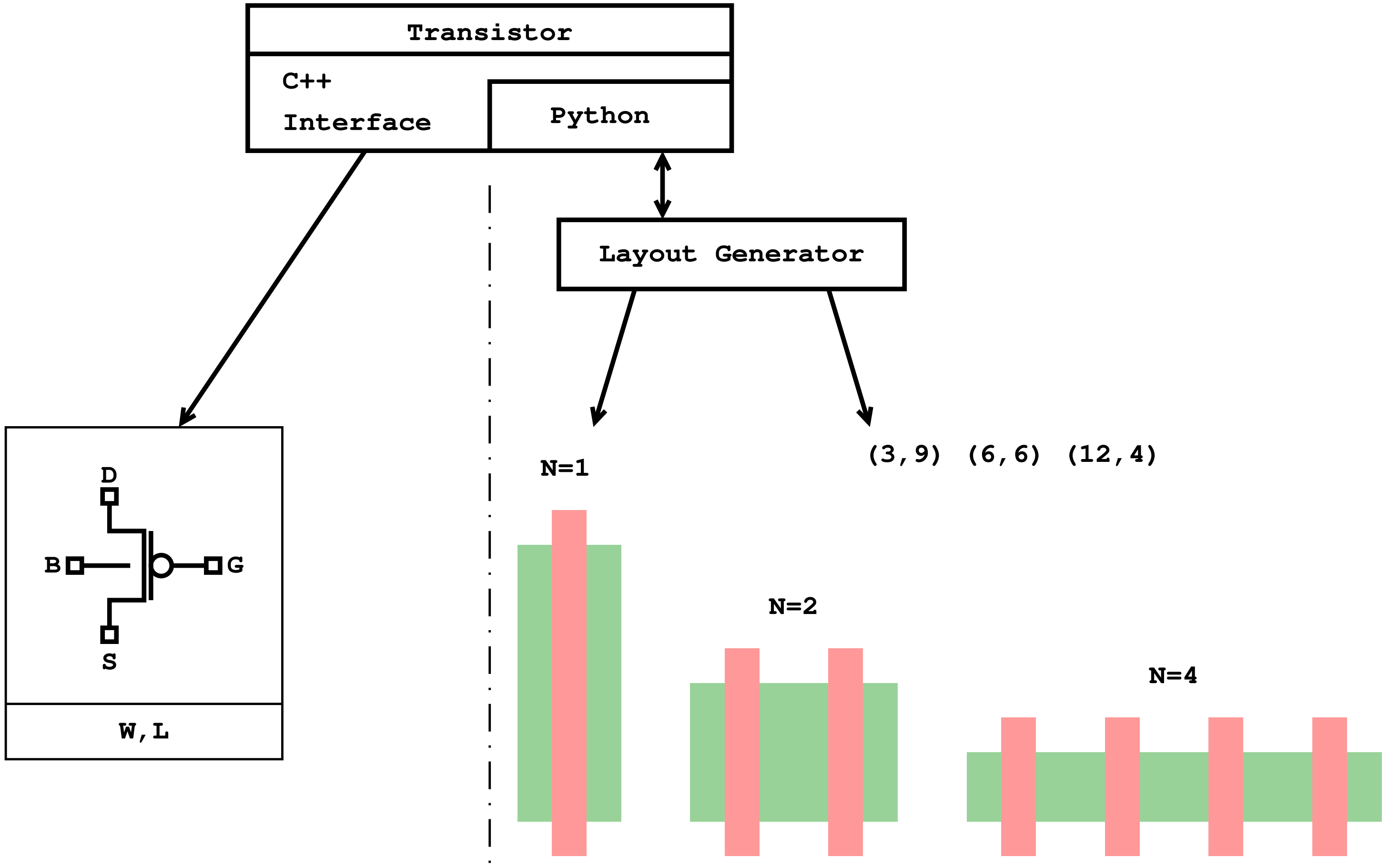
CORIOLIS – Analog Capabilities

└Analog Place & Route



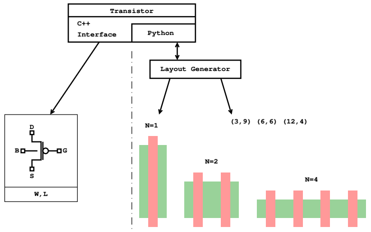
- Symmetry between two nets.
- Symmetrical lone net.
- Non-default wire width (not shown).

Devices Generators – Structure



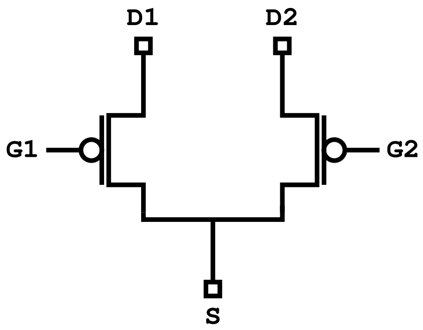
└─Devices Generators – Structure

Devices Generators – Structure

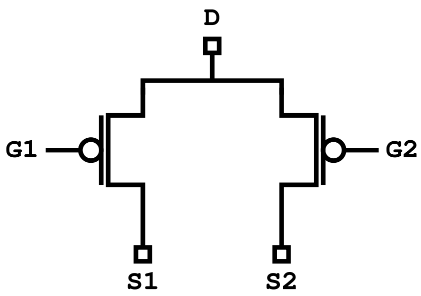


- Each device as a generator. The generator provides a fixed interface and set of parameters. W, L for transistors for instance.
- The layout is generated on demand through a user supplied Python script.
- The Python script can be written in a generic way and read the technological parameters to customize the output.
- It is a somewhat similar approach to the late Ciranova.

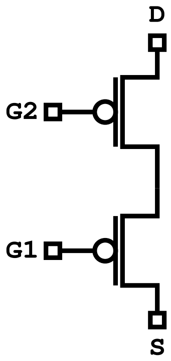
Devices Generators – Features



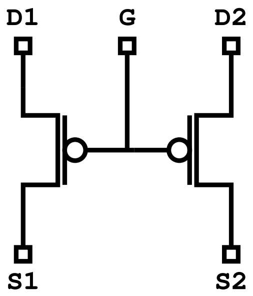
Differential pair



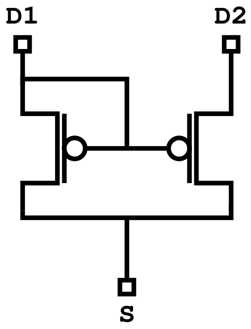
Common drain



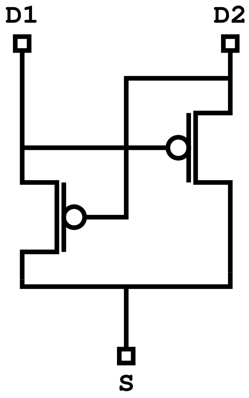
Cascode



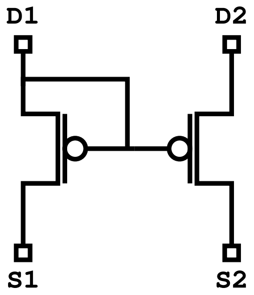
Common gate



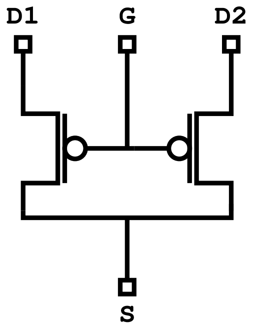
Current mirror



Crossed pair



Level shifter



Common source

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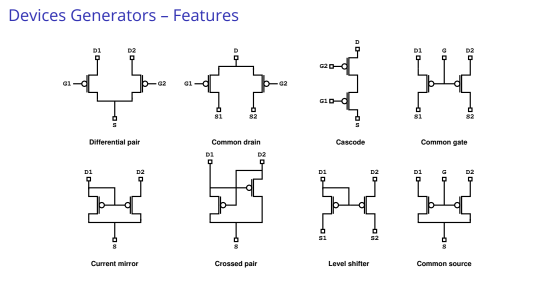
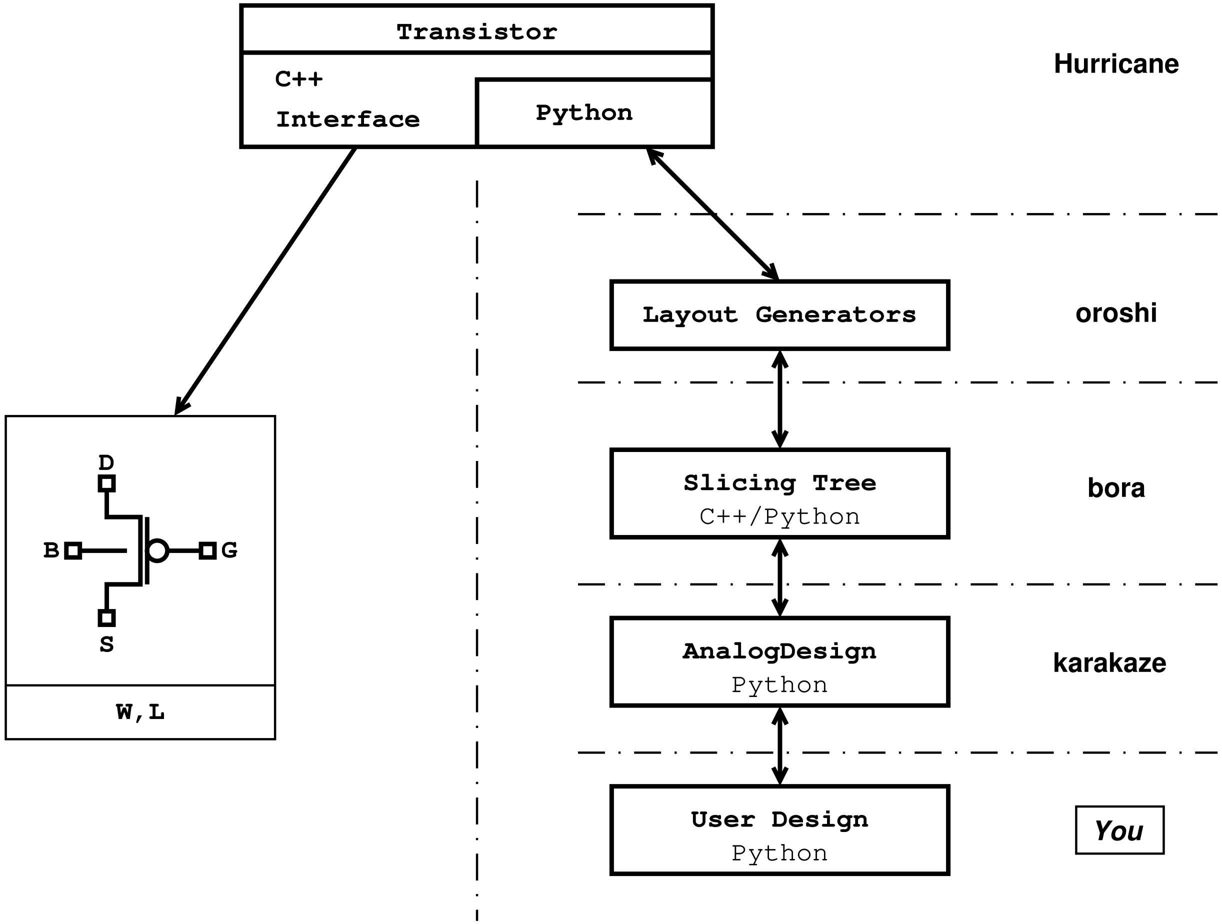
CORIOLIS – Analog Capabilities
└─Analog Place & Route
└─Devices Generators – Features


Devices Generators – Features

- More than a simple P-Cell.
- Devices generator do not only provides basic transistor, but a wide range of paired transistors.
- It is made easy because the underlying generator manages a set of fingers and their connexions.

Analog Design – Software Stack



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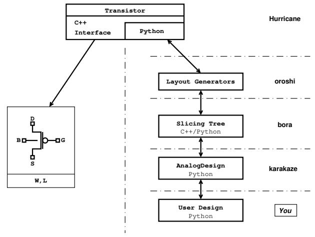
CORIOLIS – Analog Capabilities

└─Analog Place & Route

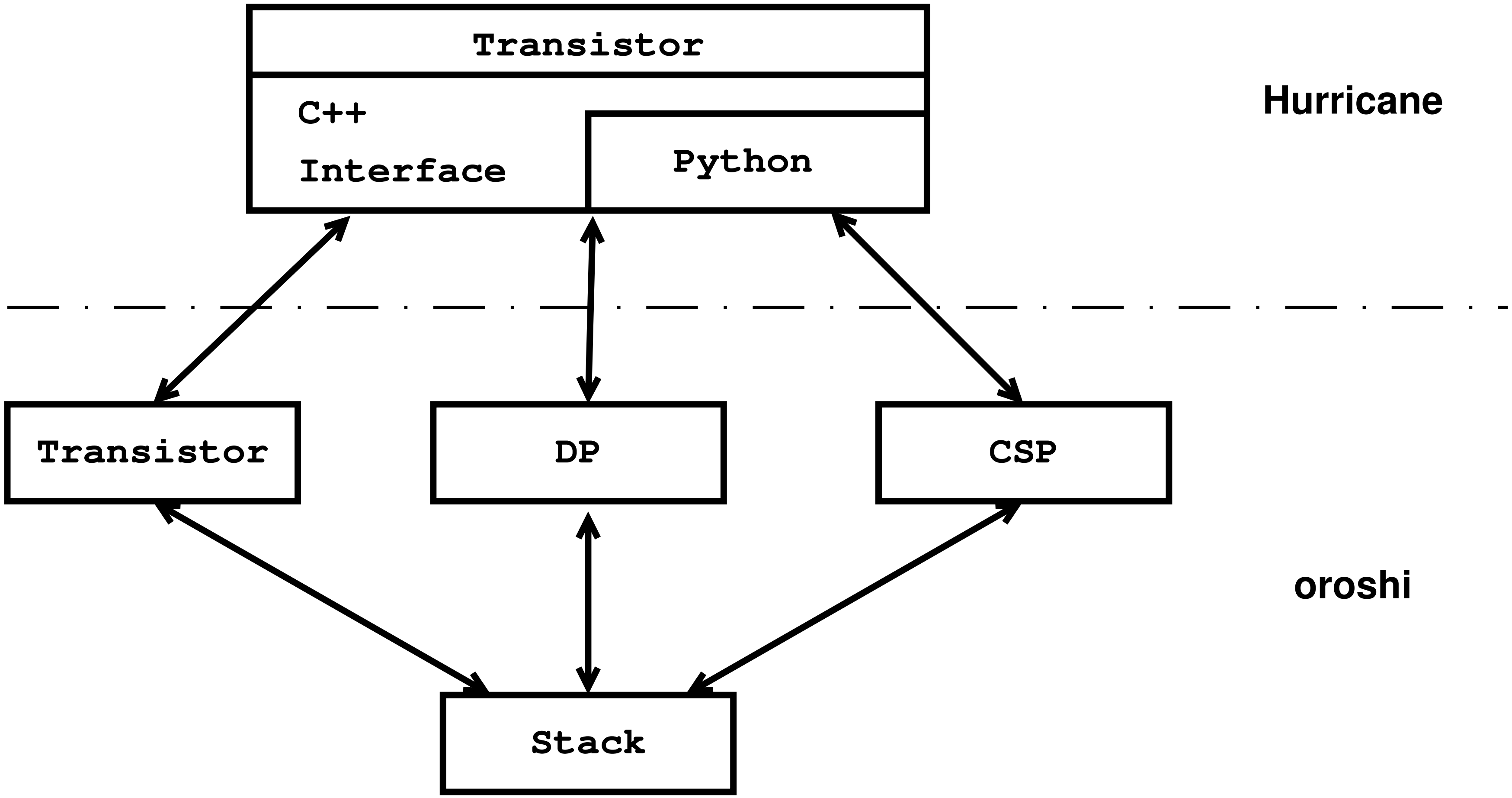
└─Analog Design – Software Stack

Analog Design – Software Stack



- A map to orient yourself in the Coriolis Deadalus.

Transistors Generators Architecture



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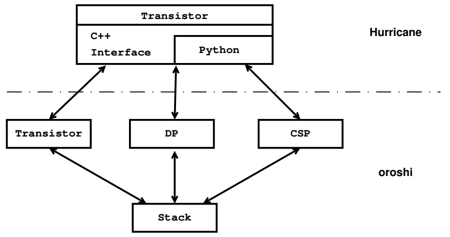
CORIOLIS – Analog Capabilities
└─Analog Place & Route

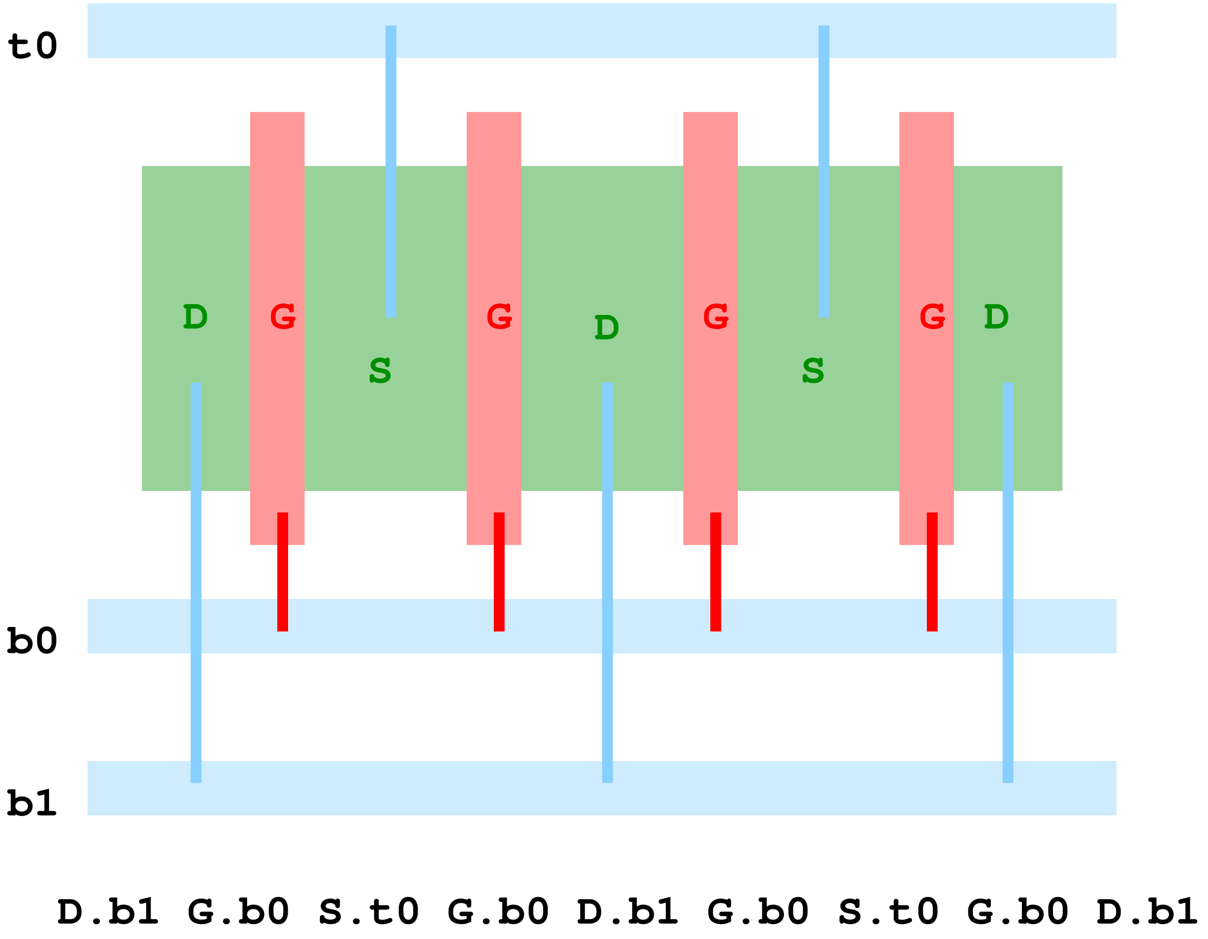
└─Transistors Generators Architecture

Transistors Generators Architecture



- As a software engineer, I take as a personal offense to have to rewrite code twice.
- The basic structure of all the paired transistors is almost the same. So we create a parametrizable generator called Stack to handle all the various cases.

The Transistor Stack Generator



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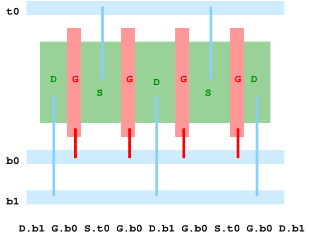
CORIOLIS – Analog Capabilities

└─Analog Place & Route

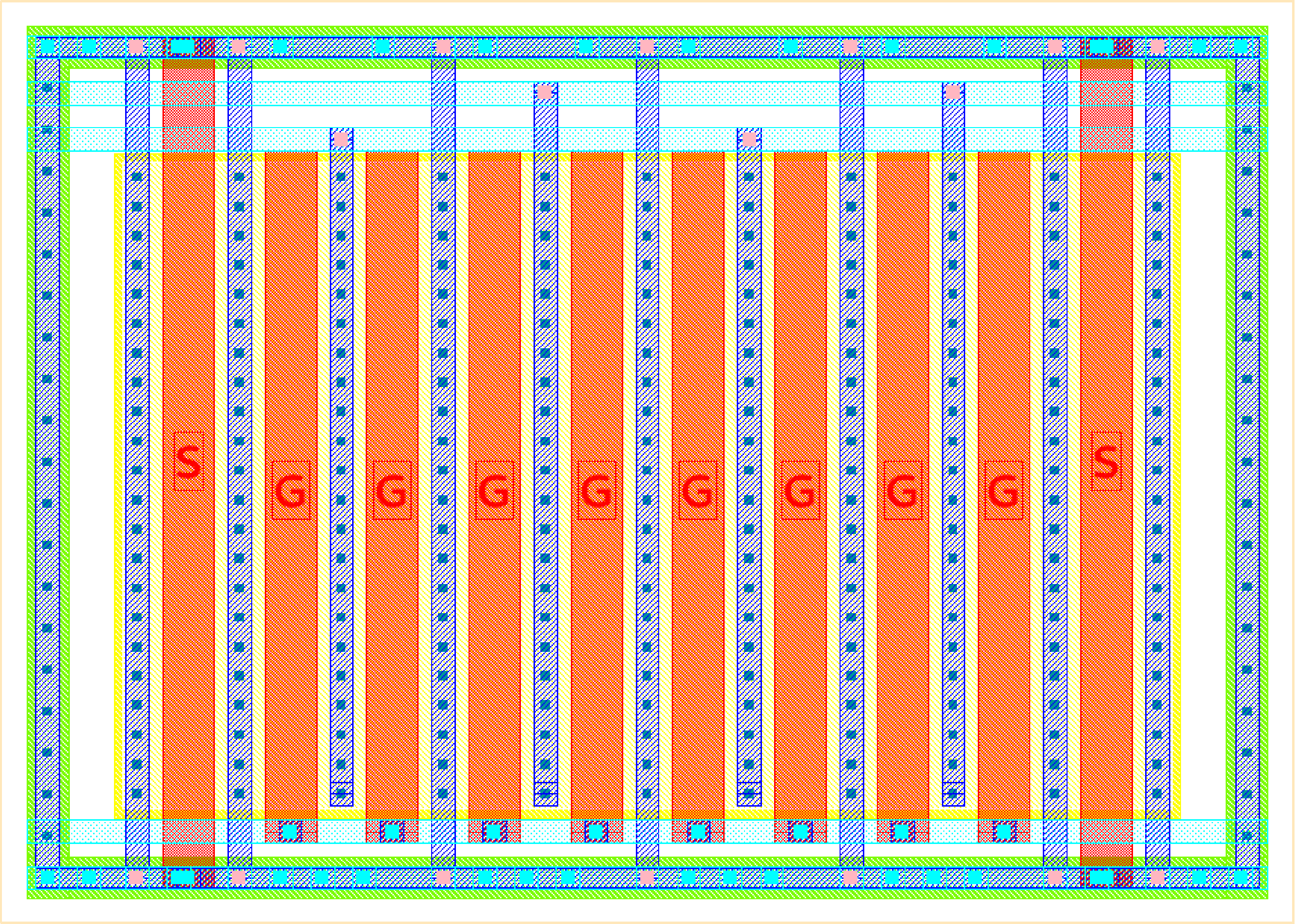
└─The Transistor Stack Generator

The Transistor Stack Generator



- The transistor stack generator is simply called with a string.

Devices Generators - Layout



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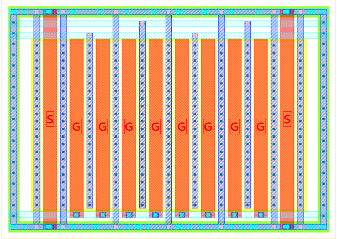
CORIOLIS – Analog Capabilities

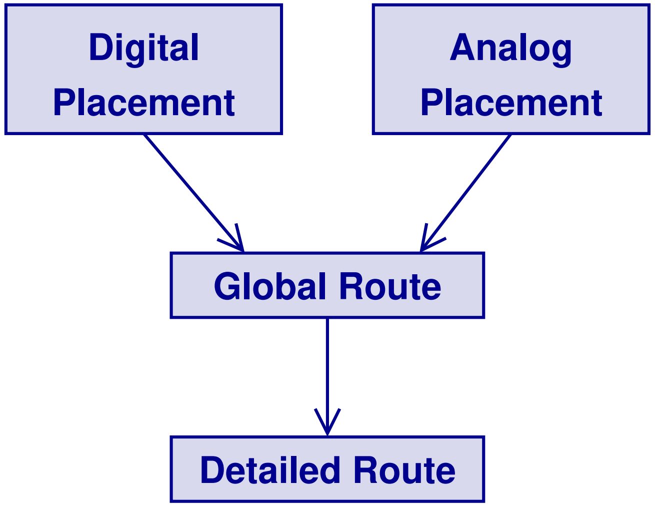
└─Analog Place & Route

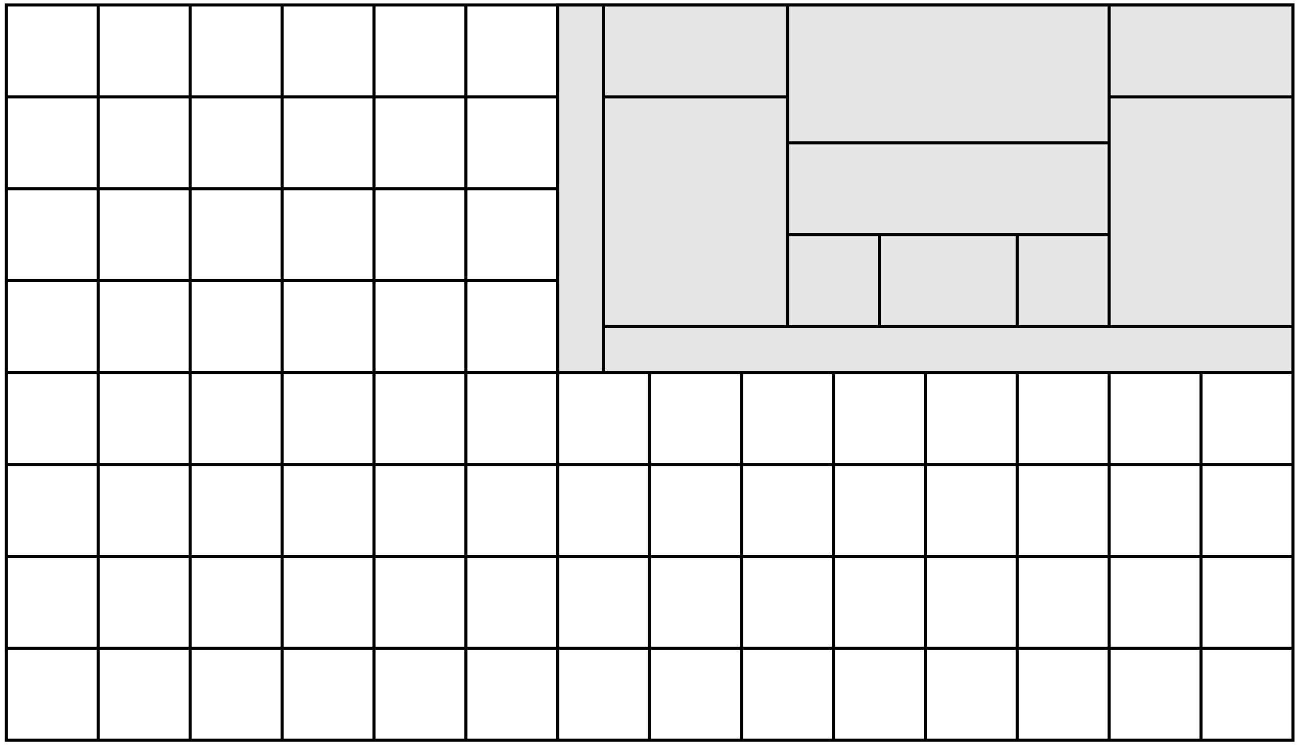
└─Devices Generators - Layout



- Here is an example of a common source pair, with dummies, source-bulk connected and a guard ring.

Support for Mixed Designs



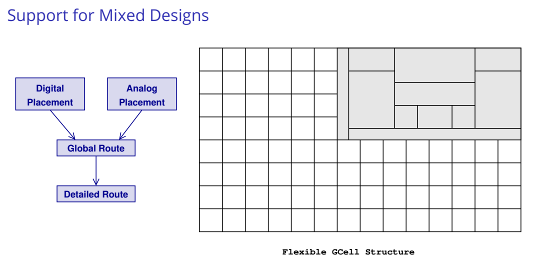


Flexible GCell Structure

CORIOLIS – Analog Capabilities

└─Analog Place & Route

└─Support for Mixed Designs



Support for Mixed Designs

- The global router GCell structure can handle configuration for both digital and analog designs. The same apply for the detailed router.
- The placement algorithms remains separates as they are quite different problems.
- Slicing tree for the analog part, regular grid for the digital part.
- So there is no longer distinctions between analog-on-top or digital-on-top.
- This is a good example of what you can achieve when you have control over the whole data-structure.

Features

- ✏ Transistor support is working.
- ✏ Capacitor and resistor Python scripts are not usable.

2025-01-25

CORIOLIS – Analog Capabilities

└─State of The Toolchain

└─Features

- The analog support was done by a PhD, but now that it has leaved, the development has stalled. Although it is maintained.
- Two internships to do the capacitors and resistors but they are not usables.
- Nesting an analog design inside a digital one is not yet implemented.

Features

- ✏ Transistor support is working.
- ✏ Capacitor and resistor Python scripts are not usable.

And now, let's have a demo…

- ✏ Using the `Gm` Chamla[1].

[1] David Chamla et al. "A Gm-C low-pass filter for zero-IF mobile applications with a very wide tuning range". In: 40.7 (July 2005), pp. 1443–1450. ISSN: 0018-9200. DOI: {10.1109/JSSC.2005.847274}.

CORIOLIS – Analog Capabilities
└─And Now, Let’s Have a Demo
└─And now, let’s have a demo…

- Show the P&R of `benchs/analog/gmChamla`.
- Show GCell grid derived from the slicing tree.
- Show a self-symmetrical net `vb5` or `vb7`.
- Show symmetrical nets `ampp_73` or `ampn_72`.
- Show symmetrical nets `m2p_in` or `m2n_in`.
- Show the P&R of `benchs/analog/gmChamlaProg`.

And now, let’s have a demo…

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