

Open Floating Point Unit

The Free IP Cores Projects
www.opencores.org

Author: Rudolf Usselmann
rudi@opencores.org

Summary:

This documents describes various building blocks for a single precision floating point unit. The minimum targeted set should include Add, Sub, Mul and Div operations. The blocks will be first presented as stand alone units, later integrated in to a single FPU block.

All source files and documents may be used and distributed without restriction provided that this copyright statement is not removed from the file and that any derivative work contains the original copyright notice and the associated disclaimer.

ALL SOURCE CODE AND DOCUMENTATION IS PROVIDED "AS IS", WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

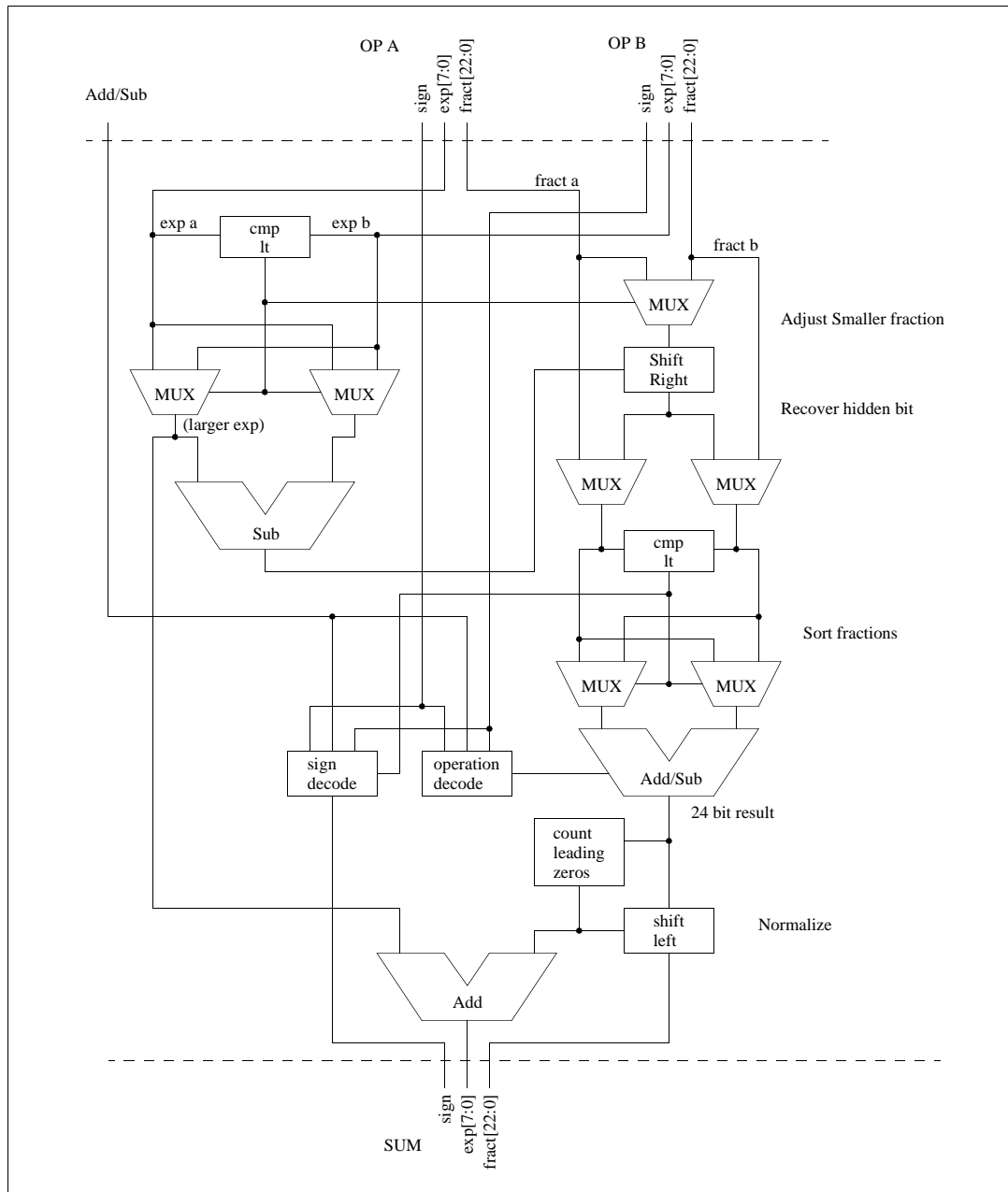
Copyright 2000 Rudolf Usselmann

1. Change Log

- 7/14/2000 RU
- Added FMUL
 - Removed Exception block (generates INF and NAN exceptions). Exceptions will be handled on a global level later on ...

2. FASU - A Floating Point Add/Subtract Unit

The FASU is a single precision floating point add/subtract unit. It is fully IEEE 754 compliant. Below diagram illustrates the internal of this implementation (pipeline not shown).



Known incompatibilities/shortcomings:

- INF and NAN might not be properly represented on the output, this will be fixed in an upper level
- Results are truncated, this should be changed to proper rounding, even though truncating is OK per IEEE

4. FDIV - A Floating Point Divide Unit