# Revision History

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# 3

# Registers

This section describes all base, control and status register inside the Ethernet IP Core.

| | | | | |
|---|---|---|---|---|
| MAC_ADDR1 | 0x12 | 32 | RW | MAC Individual Address1 |

## 3.2 INT_SOURCE (Interrupt Source Register)

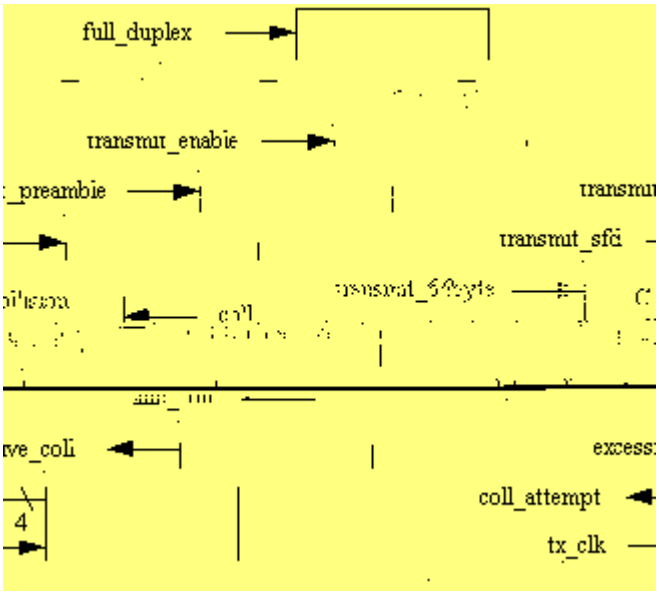
**Bit #**

| | | |
|---|---|---|
| 8 | RW | MIINOPRE – No Preamble<br>0 = 32-bit preamble send<br>1 = no preamble send |
| 7-0 | RW | CLKDIV – Clock Divider<br>The field is a host clock divider factor. The host clock can be divided |

| | | |
|---|---|---|
| 7-3 | | Reserved |
| 2 | R | SPEED<br>0 = 10 Mb/s speed<br>1 = 100 Mb/s speed |

## 4.2 TX Ethernet MAC

TX Ethernet MAC generates 10BASE-T/100BASE-TX transmit MII nibble data streams in response to the byte streams supplied from the transmit logic (host). It performs the required deferral and Backoff algorithms, takes care of the inter packet gap (IPG),


full_duplex
transmit_enable
_preamble
transmit_sfd
coll
ve_coli
excess
coll_attempt
4
tx_clk

### 5.2.8 Jam Timer

The function of this module is to determine how long JAM pattern has been transmitted after a collision.

21.3.2001

[redacted]

### 5.5.1 Operation Control Module

The function of this module is to perBT2the iowingy commands: Tj /TF 1 Tf 1.44 0 TD 0 TW-6.95ryite c
TFigure 5:OperM-108.2l

### 5.5.2 Output Control Module

Controls the signal appearance on the MDO, MCK and MDOEN pins.

Reset

BitCounter

**Figure 6: Output Control Module**

### 5.5.3 Shift Register

Holds the status read from an external PHY.

**Figure 7: Shift Register**

### 5.5.4 Clock Generator

Generates an appropriate output clock MCK according to the input host clock and the clock divider bits (CLKDIV[7:0] in the MIIMODER register).

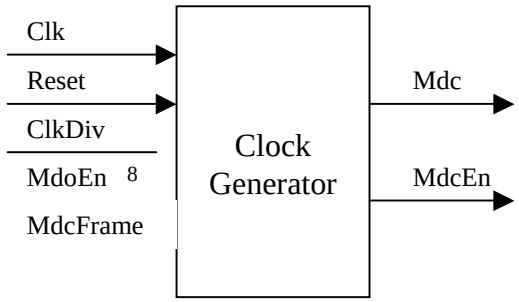



**Figure 8: Clock Generator**